

CLAIMS

1. An apparatus comprising:

a plurality of logic modules, each logic module being configured to selectively process image related data according to a different image processing
5 algorithm; and

communication logic operatively coupled to each of the logic modules and configured to selectively route the image related data to the plurality of logic modules for processing in accordance with a data processing order.

10 2. The apparatus as recited in Claim 1, wherein the communication logic includes:

a plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module; and

a plurality of buses, operatively coupled to route the image related data
15 between the plurality of bus interfaces.

3. The apparatus as recited in Claim 2, wherein the plurality of buses includes at least one memory bus and at least one support bus, and further comprising a memory bus interface operatively coupled to the memory
20 bus.

4. The apparatus as recited in Claim 3, wherein the memory bus interface is further configured as a memory controller and configurable for use with memory.
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5. The apparatus as recited in Claim 4, further comprising memory operatively coupled to the memory bus interface.

6. The apparatus as recited in Claim 5, wherein the memory bus is configured to selectively route the image related data between the memory and at least one of the plurality of logic modules via the bus interface associated with the at least one logic module and the memory bus interface.

7. The apparatus as recited in Claim 3, wherein the support bus is configured to selectively route the image related data between at least two of the plurality of logic modules via the two bus interfaces associated with the at least two logic modules.

8. The apparatus as recited in Claim 1, wherein at least a portion of the plurality of logic modules are configured to share information with other logic modules through the communication logic.

9. The apparatus as recited in Claim 8, wherein the portion of the plurality of logic modules are configured to share information with other logic modules by sending and receiving one or more messages via the communication logic.

10. The apparatus as recited in Claim 9, wherein the message includes at least one identifier selected from a group of identifiers comprising a destination identifier, a source identifier, and a bus identifier.

11. The apparatus as recited in Claim 9, wherein the message includes a data field capable of carrying the image related data.

12. The apparatus as recited in Claim 11, wherein the image related data carried in the data field of the message includes at least one form of data selected from a group of data comprising image data, index data, and address data.

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13. The apparatus as recited in Claim 1, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning
10 algorithm, a filtering algorithm, a convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

14. The apparatus as recited in Claim 1, wherein the data processing order is associated with an image processing pipeline.

15. The apparatus as recited in Claim 2, wherein the data processing order is established via control inputs to the plurality of bus interfaces.

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16. An apparatus comprising:
a plurality of logic modules, each logic module being configured to selectively process image related data according to a different image processing algorithm;
25 a plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module; and

a plurality of buses, operatively coupled to the plurality of bus interfaces, and wherein the plurality of bus interfaces are configurable to selectively route image related data through the plurality of buses to the plurality of logic modules for processing in accordance with a programmable
5 data processing order.

17. The apparatus as recited in Claim 16, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data.

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18. The apparatus as recited in Claim 16, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning
15 algorithm, a filtering algorithm, a convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

20 19. The apparatus as recited in Claim 17, wherein the programmable data processing order causes an image processing pipeline to be formed using at least a portion of the plurality of logic modules.

20. An image processing device comprising:
25 a memory bus;
at least one support bus;
memory suitable for storing image related data;

a memory bus interface coupled to the memory bus and the memory and configured to provide access to the memory via the memory bus;

a plurality of logic modules, each logic module being configured to process image related data according to a different image processing algorithm;

5 and

a plurality of bus interfaces, each bus interface being coupled to a corresponding logic module, the support bus and the memory bus, and configurable to selectively route the image related data through the support bus and the memory bus to the plurality of logic modules for processing in accordance with a data processing order.

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21. The image processing device as recited in Claim 20, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data.

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22. The image processing device as recited in Claim 20, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning algorithm, a filtering algorithm, a convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

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23. The apparatus as recited in Claim 20, wherein the data processing order causes an image processing pipeline to be formed using at least a portion of the plurality of logic modules.

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24. The apparatus as recited in Claim 20, wherein the data processing order is established via control inputs to the plurality of bus interfaces.

5 25. The image processing device as recited in Claim 20, wherein the image processing device is selected from a group of image processing devices comprising a color printing device, monochrome printing device, an image scanning device, a facsimile device, an image copying device, an image reproduction device, and image displaying device, an image generating device,
10 an image capturing device a still camera device, and a video camera device.